NCV7321

Stand Alone LIN Transceiver

Description

The NCV7321 is a fully featured local interconnect network (LIN) transceiver designed to interface between a LIN protocol controller and the physical bus. The transceiver is implemented in I3T technology enabling both high−voltage analog circuitry and digital functionality to co−exist on the same chip.

The NCV7321 LIN device is a member of the in−vehicle networking (IVN) transceiver family. It is designed to work in harsh automotive environment and is submitted to the TS16949 qualification flow.

The LIN bus is designed to communicate low rate data from control devices such as door locks, mirrors, car seats, and sunroofs at the lowest possible cost. The bus is designed to eliminate as much wiring as possible and is implemented using a single wire in each node. Each node has a slave MCU−state machine that recognizes and translates the instructions specific to that function. The main attraction of the LIN bus is that all the functions are not time critical and usually relate to passenger comfort.

Features

- General
  - SOIC−8 Green package (Pb−Free)
- LIN−Bus Transceiver
  - LIN Compliant to Specification Revision 2.0 and 2.1 (Backwards Compatible to Version 1.3) and J2602
  - Bus Voltage ±45 V
  - Transmission Rate 1 kbps to 20 kbps
- Protection
  - Thermal Shutdown
  - Indefinite Short−Circuit Protection on Pins LIN and WAKE Towards Supply and Ground
  - Load Dump Protection (45 V)
  - Bus Pins Protected Against Transients in an Automotive Environment
- EMI Compatibility
  - Integrated Slope Control
- Modes
  - Normal Mode: LIN Transceiver Enabled, Communication via the LIN Bus is Possible, INH Switch is On
  - Sleep Mode: LIN Transceiver Disabled, the Consumption from V_{BB} is Minimized, INH Switch is Off
  - Standby Mode: transition mode reached either after power−up or after a wakeup event, INH switch is on
  - Wake−up Bringing the Component from Sleep Mode into Standby Mode is Possible either by LIN Command, a Digital Signal on WAKE Pin (e.g. External Switch) or Directly via EN pin.

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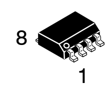
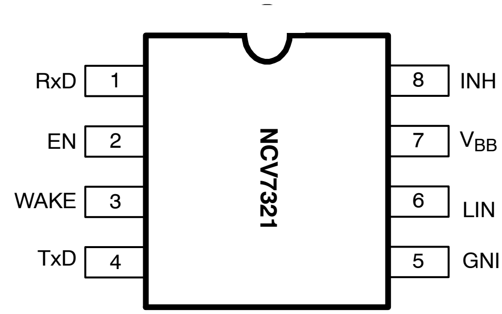


SOIC−8
CASE 751

PIN ASSIGNMENT



(Top View) PC20040918.3

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

KEY TECHNICAL CHARACTERISTICS AND OPERATING RANGES

Table 1. TECHNICAL CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit
V_{BB}	Nominal Battery Operating Voltage (Note 1)	5	12	27	V
	Load Dump Protection (Note 2)			45	
I_{BB}_SLP	Supply Current in Sleep Mode			20	μA
V_{WAKE}	Operating DC Voltage on WAKE Pin	0		V_{BB}	V
	Maximum Rating Voltage on WAKE Pin	−45		45	V
V_{INH}	Operating DC Voltage on INH Pin	0		V_{BB}	V
V_Dig_IO	Operating DC Voltage on Digital IO Pins (EN, RxD, TxD)	0		5.5	V
T_J	Junction Thermal Shutdown Temperature		165		°C
T_{amb}	Operating Ambient Temperature	−40		+125	°C
V_{ESD}	Electrostatic Discharge Voltage (LIN, WAKE, V_{BB}) System Human Body Model for NCV7321−0 (Note 3)	−5		+5	kV
	Electrostatic Discharge Voltage (LIN, WAKE, V_{BB}) System Human Body Model for NCV7321−1 (Note 3)	−6		+6	
	Electrostatic Discharge Voltage (all pins) Human Body Model (Note 4)	−4		+4	

1. Below 5 V on V_{BB} in normal mode, the bus will either stay recessive or comply with the voltage level specifications and transition time specifications as required by SAE J2602. It is ensured by the battery monitoring circuit (see par. 7.2.3).
2. The applied transients shall be in accordance with ISO 7637 part 1, test pulse 5. The device complies with functional class C; class A can be reached depending on the application and external components.
3. Equivalent to discharging a 150 pF capacitor through a 330 Ω resistor conform to IEC Standard 1000−4−2. Additional external protection components might be needed to reach the specified system ESD levels depending on the application. WAKE pin is stressed through a 33 kΩ resistor.
4. Equivalent to discharging a 100 pF capacitor through a 1.5k Ω resistor conform to MIL STD 883 method 3015.7.

BLOCK DIAGRAM

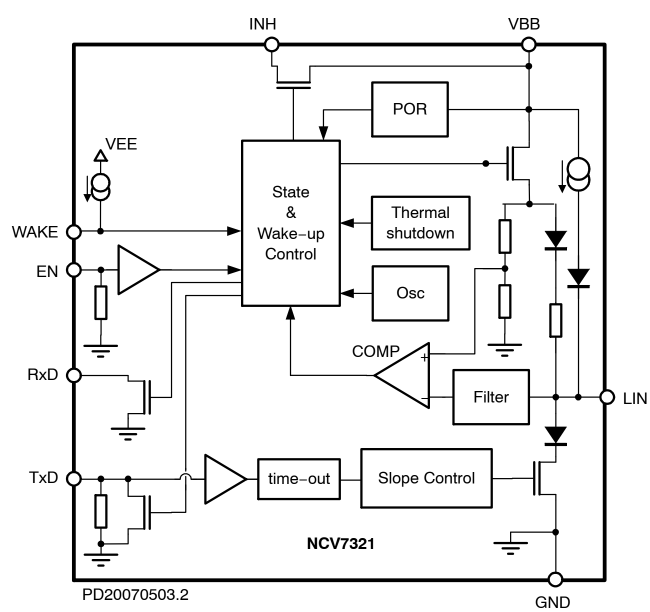


Figure 1. Block Diagram

TYPICAL APPLICATION

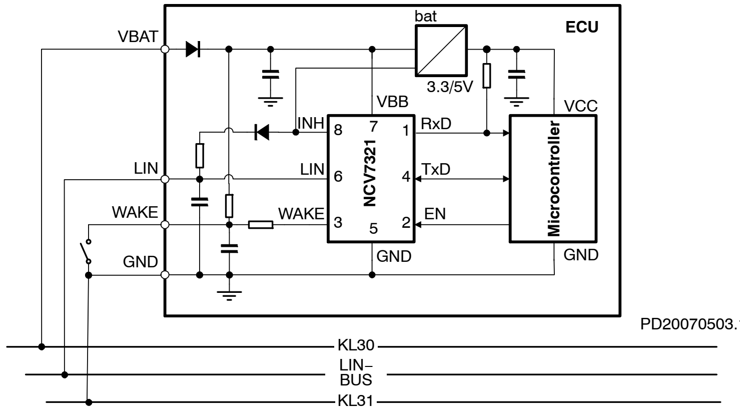


Figure 2. Typical Application Diagram for a Master Node

Table 2. PIN DESCRIPTION

Pin	Name	Description
1	RxD	Receive Data Output; Low in Dominant State; Open−Drain Output
2	EN	Enable Input, Transceiver in Normal Operation Mode when High, Pulldown Resistor to GND
3	WAKE	High Voltage Digital Input Pin to Apply Local Wakeup, Sensitive to Falling Edge, Pullup Current Source to V_{BB}
4	TxD	Transmit Data Input, Low for Dominant State, Pulldown to GND (Switchable Strength for Wakeup Source Recognition)
5	GND	Ground
6	LIN	LIN Bus Output/Input
7	V_{BB}	Battery Supply Input
8	INH	Inhibit Output, Switch Between INH and V_{BB} can be Used to Control External Regulator or Pullup Resistor on LIN Bus

Table 3. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
V_{BB}	Battery Voltage on Pin V_{BB} (Note 5)	−0.3	+45	V
V_{LIN}	LIN Bus Voltage (Note 6)	−45	+45	V
V_{INH}	DC Voltage on inhibit Pin	−0.3	V_{BB} + 0.3	V
V_{WAKE}	DC Voltage on WAKE Pin	−35	45	V
V_Dig_IO	DC Input Voltage on Pins TxD, RxD, and EN	−0.3	7	V
T_J	Maximum Junction Temperature	−40	+150	°C
V_{ESD}	Electrostatic Discharge Voltage (Pins LIN, WAKE and V_{BB}) System Human Body Model for NCV7321−0 (Note 7)	−5	+5	kV
	Electrostatic Discharge Voltage (Pins LIN, WAKE and V_{BB}) System Human Body Model for NCV7321−1 (Note 7)	−6	+6	
	Electrostatic Discharge Voltage (All Pins) Human Body Model (Note 8)	−4	+4	
	Electrostatic Discharge Voltage; Charge Device Model (Note 9)	−500	+500	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

5. The applied transients shall be in accordance with ISO 7637 part 1, test pulses 1, 2, 3a, 3b, and 5. The device complies with functional class C; class A can be reached depending on the application and external components.
6. The applied transients shall be in accordance with ISO 7637 part 1, test pulses 1, 2, 3a, and 3b. The device complies with functional class C; class A can be reached depending on the application and external components.
7. Equivalent to discharging a 150 pF capacitor through a 330 Ω resistor conform to IEC Standard 1000−4−2. Additional external protection components might be needed to reach the specified system ESD levels depending on the application. WAKE pin is stressed through a 33 kΩ resistor.
8. Equivalent to discharging a 100 pF capacitor through a 1.5kΩ resistor conform to MIL STD 883 method 3015.7.
9. Conform to EOS/ESD−DS5.3 (socketed mode).

FUNCTIONAL DESCRIPTION

Overall Functional Description

LIN is a serial communication protocol that efficiently supports the control of mechatronic nodes in distributed automotive applications. The domain is class−A multiplex buses with a single master node and a set of slave nodes.

The NCV7321 contains the LIN transmitter, LIN receiver, power−on−reset (POR) circuits and thermal shutdown (TSD). The LIN transmitter is optimized for the maximum specified transmission speed of 20 kB with EMC performance due to reduced slew rate of the LIN output.

The junction temperature is monitored via a thermal shutdown circuit that switches the LIN transmitter off when temperature exceeds the TSD trigger level.

The NCV7321 has four operating states (unpowered mode, standby mode, normal mode and sleep mode) that are determined by the supply voltage V_{BB}, input signals EN and WAKE and activity on the LIN bus.

OPERATING STATES

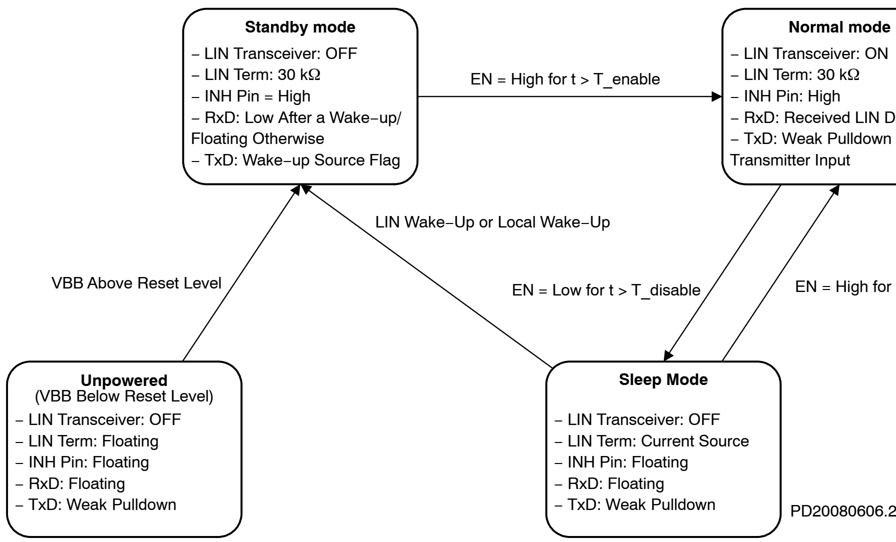


Figure 3. State Diagram

Unpowered Mode

As long as V_{BB} remains below its power−on−reset level, the chip is kept in a safe unpowered state. LIN transmitter is inactive, both LIN and INH pins are left floating and only a weak pulldown is connected on pin TxD. Pin RxD remains floating.

The unpowered state will be entered from any other state when V_{BB} falls below its power−on−reset level.

Standby Mode

Standby mode is a low−power mode, where LIN transceiver remains inactive while INH pin is driven high to activate an external voltage regulator – see Figure 2. Depending on the transition which led to the standby mode, pins RxD and TxD are configured differently during this mode. A 30 kΩ resistor in series with a reverse−protection diode is internally connected between LIN and V_{BB} Pins.

Standby mode is entered in one of the following ways:

- After the voltage level at V_{BB} pin rises above its power−on−reset level. In this case, RxD Pin remains high−impedant and the pulldown applied on pin TxD remains weak.
- After a wakeup event is recognized while the chip was in the sleep mode. Pin RxD is pulled low while pin TxD signals the type of wakeup leading to the standby mode – its pullup remains weak for LIN wakeup and it is switched to strong pulldown for the case of local wakeup (i.e. wakeup via Pin WAKE).

While in the standby mode, the configuration of Pins RxD and TxD remains unchanged, regardless the activity on WAKE and LIN Pins – i.e. if additional wakeups occur during the standby mode, they have no influence on the chip configuration.

Normal Mode

In normal mode, the full functionality of the LIN transceiver is available. Data according the state of TxD input are sent to the LIN bus while pin RxD reflects the logical symbol received on the LIN bus – high−impedant for recessive and Low for dominant. A 30 kΩ resistor in series with a reverse−protection diode is internally connected between LIN and V_{BB} pins.

To avoid that, due to a failure of the application (e.g. software error), the LIN bus is permanently driven dominant and thus blocking all subsequent communication, signal on pin TxD passes through a timer, which releases the bus in case TxD remains low for longer than T_TxD_timeout. The transmission can continue once the TxD returns to High logical level.

In case the junction temperature increases above the thermal shutdown threshold, e.g. due to a short of the LIN wiring to the battery, the transmitter is disabled and releases LIN bus to recessive. Once the junction temperature decreases back below the thermal shutdown release level, the transmission can be enabled again – however, to avoid thermal oscillations, first a High logical level on TxD must be encountered before the transmitter is enabled.

As required by SAE J2602, the transceiver must behave safely below its operating range – it shall either continue to transmit correctly (according its specification) or remain silent (transmit a recessive state regardless the of the TxD signal). A battery monitoring circuit in NCV7321 de−activates the transmitter in the normal mode if the V_{BB} level drops below MONL_V_{BB}. Transmission is enabled again when V_{BB} reaches MONH_V_{BB}. The internal logic remains in the normal mode and the reception from the LIN line is still possible even if the battery monitor disables the transmission. Although the specifications of the monitoring and power−on−reset levels are overlapping, it's ensured by the implementation that the monitoring level never falls below the power−on−reset level.

Normal mode can be entered from either standby or sleep mode when EN Pin is High for longer than T_enable. When the transition is made from standby mode, TxD pulldown is set to weak and RxD is put high−impedant immediately after EN becomes High (before the expiration of T_enable filtering time). This excludes signal conflicts between the standby mode pin settings and the signals required to control the chip in the normal mode (e.g. strong pull−down on TxD after local wakeup vs. High logical level on TxD required to send a recessive symbol on LIN).

Sleep Mode

Sleep mode provides extremely low current consumption. The LIN transceiver is inactive and the battery consumption is minimized. Pin INH is put to high−impedant state to disable the external regulator and, in case of a master node, the LIN termination – see Figure 2. Only a weak pullup current source is internally connected between LIN and V_{BB} Pins, in order to minimize current consumption even in case of LIN short to GND.

Sleep mode can be entered from normal mode by assigning Low logical level to pin EN for longer than T_disable. The sleepmode can be entered even if a permanent short occurs either on LIN or WAKE Pin.

If a wakeup event occurs during the transition between normal and sleep mode (during the T_disable filtering time), it will be regarded as valid wakeup and the chip will enter standby mode with the appropriate setting of Pins RxD and TxD.

Wake−up

Two types of wakeup events are recognized by NCV7321:

- Local wakeup – when a high−to−low transition on pin WAKE is encountered and WAKE pin remains Low at least during T_WAKE – see Figure 5.
- Different threshold parameters apply compared to the receiver in the normal mode (see parameters Vrec_rec_slp and Vrec_hys_slp)

Wakeup events can be exclusively detected in sleep mode or during the transition from normal mode to sleep mode. Due to timing tolerances, valid wakeup events beginning shortly before normal−to−sleep mode transition can be also sometimes regarded as valid wakeups.

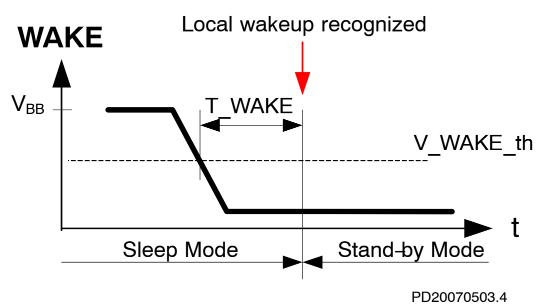


Figure 4. Local Wakeup Detection

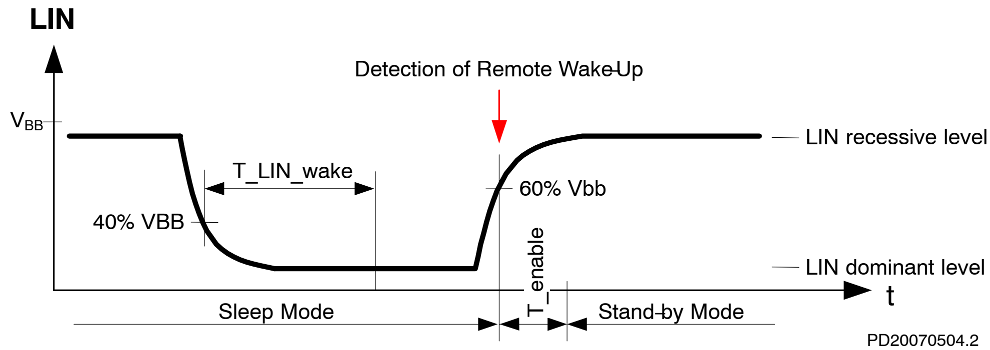


Figure 5. Remote (LIN) Wakeup Detection

ELECTRICAL CHARACTERISTICS

Definitions

All voltages are referenced to GND (Pin 5). Positive currents flow into the IC.

Table 4. DC CHARACTERISTICS (V_{BB} = 5 V to 27 V; T_J = −40°C to +150°C; unless otherwise specified. Typical values are given at V(V_{BB}) = 12 V and T_J = 25°C, unless specified otherwise.)

DC CHARACTERISTICS – SUPPLY

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BB}						
I_{BB}_ON_rec	V_{BB} Consumption	Normal Mode; LIN recessive V_{LIN} = V(V_{BB}) = V_{INH} = V_{WAKE}			1.6	mA
I_{BB}_ON_dom	V_{BB} Consumption	Normal Mode; LIN dominant V(V_{BB}) = V_{INH} = V_{WAKE}			8	mA
I_{BB}_STB	V_{BB} Consumption	Standby Mode V_{LIN} = V(V_{BB}) = V_{INH} = V_{WAKE}			350	μA
I_{BB}_SLP	V_{BB} Consumption	Sleep Mode V_{LIN} = V(V_{BB}) = V_{INH} = V_{WAKE}			30	μA
I_{BB}_SLP_18V	V_{BB} Consumption	Sleep Mode, V_{BB} < 18 V V_{LIN} = V(V_{BB}) = V_{INH} = V_{WAKE}			20	μA
I_{BB}_SLP_12V	V_{BB} Consumption	Sleep Mode, V_{BB} = 12 V, T_J < 85°C V_{LIN} = V(V_{BB}) = V_{INH} = V_{WAKE}			10	μA
LIN TRANSMITTER						
VLIN_dom_LoSup	LIN Dominant Output Voltage	TXD = Low; V_{BB} = 7.3 V			1.2	V
VLIN_dom_HiSup	LIN Dominant Output Voltage	TXD = Low; V_{BB} = 18 V			2.0	V
VLIN_REC	LIN Recessive Output Voltage	TXD = HighH; I_{LIN} = 0 mA	V_{BB} – Vγ (Note 10)			V
ILIN_lim	Short Circuit Current Limitation	V_{LIN} = V_{BB}_max	40		200	mA
R_{slave}	Internal Pullup Resistance		20	33	47	kΩ
ILIN_off_dom	LIN output current, bus in dominant state	Normal Mode, Driver Off; V_{BB} = 12 V	−1			mA
ILIN_off_dom_slp	LIN Output Current, Bus in Dominant State	Sleep Mode, Driver Off; V_{BB} = 12 V	−20	−15	−2	μA

10. Vγ is the forward diode voltage. Typically (over the complete temperature) Vγ = 1 V.

Table 4. DC CHARACTERISTICS (V_{BB} = 5 V to 27 V; T_J = −40°C to +150°C; unless otherwise specified. Typical values are given at V(V_{BB}) = 12 V and T_J = 25°C, unless specified otherwise.)

DC CHARACTERISTICS – SUPPLY

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LIN TRANSMITTER						
ILIN_off_rec	LIN Output Current, Bus in Recessive State	Driver Off; V_{BB} = 12 V			5	μA
ILIN_no_GND	Communication not Affected	V_{BB} = GND = 12 V; 0 < V_{LIN} < 18 V	−1		1	mA
ILIN_no_V_{BB}	LIN Bus Remains Operational	V_{BB} = GND = 0 V; 0 < V_{LIN} < 18 V			100	μA
LIN RECEIVER						
Vrec_dom	Receiver Threshold	LIN Bus Recessive – Dominant	0.4		0.5	V_{BB}
Vrec_rec	Receiver Threshold	LIN Bus Dominant – Recessive	0.5		0.6	V_{BB}
Vrec_cnt	Receiver Centre Voltage	(Vbus_dom + Vbus_rec)/2	0.475		0.525	V_{BB}
Vrec_hys	Receiver Hysteresis	(Vbus_rec – Vbus_dom)	0.05		0.175	V_{BB}

DC CHARACTERISTICS – I/Os

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PIN EN						
Vil_EN	Low Level Input Voltage		−0.3		0.8	V
Vih_EN	High Level Input Voltage		2.0		5.5	V
Rpd_EN	Pulldown Resistance to Ground (Note 10)		150	350	650	kΩ
PIN INH						
Delta_VH	High Level Voltage Drop	I_{INH} = 15 mA, INH Active	0.1	0.35	0.75	V
I_leak	Leakage Current	Sleep Mode; V_{INH} = 0 V	−1	0	1	μA
PIN RxD						
Iol_RxD	Low Level Output Current	V_{RxD} = 0.4 V, normal mode, V_{LIN} = 0 V	1.5			mA
Ioh_RxD	High Level Output Current	V_{RxD} = 5 V, Normal Mode, V_{LIN} = V(V_{BB})	−5	0	5	μA
PINS TxD						
Vil_TxD	Low Level Input Voltage		−0.3		0.8	V
Vih_TxD	High Level Input Voltage		2.0		5.5	V
Rpd_TxD	Pulldown Resistor on TxD Pin, Corresponding to “Weak Pulldown”	Normal Mode or Sleep Mode or Standby Mode after Powerup or Standby Mode after LIN Wakeup	150	350	650	kΩ
Ipd_RxD_Strong	Pulldown Current on TxD Pin Corresponding to “Strong Pulldown”	Standby Mode after Local Wakeup	1.5			mA

10. $V\gamma$ is the forward diode voltage. Typically (over the complete temperature) $V\gamma$ = 1 V.

Table 4. DC CHARACTERISTICS (V_{BB} = 5 V to 27 V; T_J = −40°C to +150°C; unless otherwise specified. Typical values are given at V(V_{BB}) = 12 V and T_J = 25°C, unless specified otherwise.)

DC CHARACTERISTICS – I/Os

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PIN WAKE						
V_wake_th	WAKE Threshold Voltage		V_{BB} – 3.3		V_{BB} – 1.1	V
I_wake_pullup	Pullup Current on Pin WAKE	V_{WAKE} = 0 V	−30	−15	−1	μA
I_wake_leak	Leakage of Pin WAKE	V_{WAKE} = V(V_{BB})	−5	0	5	μA

DC CHARACTERISTICS – POWER−ON−RESET, BATTERY MONITORING AND THERMAL SHUTDOWN

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
POR AND V_{BB} MONITOR						
PORH_V_{BB}	Power−on Reset High Level on V_{BB}	V_{BB} Rising	2		4.5	V
PORL_V_{BB}	Power−on Reset Low Level on V_{BB}	V_{BB} Falling	1.7		4	V
MONH_V_{BB}	Battery Monitoring High Level	V_{BB} Rising			4.5	
MONL_V_{BB}	Battery Monitoring Low Level	V_{BB} Falling	3			
TSD						
T_J	Junction Temperature	Temperature Rising		165		°C
T_J_hyst	Thermal Shutdown Hysteresis		9		18	°C

10. Vγ is the forward diode voltage. Typically (over the complete temperature) Vγ = 1 V.

Table 5. AC CHARACTERISTICS V_{BB} = 5 V to 27 V; T_J = −40°C to +150°C; unless otherwise specified. For the transmitter parameters, the following bus loads are considered: L1 = 1 kΩ / 1 nF; L2 = 660 Ω / 6.8 nF; L3 = 500 Ω / 10 nF

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
LIN TRANSMITTER						
D1	Duty Cycle 1 = $t_{BUS\_REC(min)}$ / (2 x T_{Bit})	$TH_{REC(min)}$ = 0.744 x V_{BB} $TH_{DOM(min)}$ = 0.581 x V_{BB} T_{BIT} = 50 μs V(V_{BB}) = 7 V to 18 V	0.396		0.5	
D2	Duty Cycle 2 = $t_{BUS\_REC(max)}$ / (2 x T_{Bit})	$TH_{REC(max)}$ = 0.422 x V_{BB} $TH_{DOM(max)}$ = 0.284 x V_{BB} T_{BIT} = 50 μs V(V_{BB}) = 7.6 V to 18 V	0.5		0.581	
D3	Duty Cycle 3 = $t_{BUS\_REC(min)}$ / (2 x T_{Bit})	$TH_{REC(min)}$ = 0.788 x V_{BB} $TH_{DOM(min)}$ = 0.616 x V_{BB} T_{BIT} = 96 μs V(V_{BB}) = 7 V to 18 V	0.417		0.5	
D4	Duty Cycle 4 = $t_{BUS\_REC(max)}$ / (2 x T_{Bit})	$TH_{REC(max)}$ = 0.389 x V_{BB} $TH_{DOM(max)}$ = 0.251 x V_{BB} T_{BIT} = 96 μs V(V_{BB}) = 7.6 V to 18 V	0.5		0.590	
T_fall	LIN Falling Edge	Normal Mode; V_{BB} = 12 V			22.5	μs
T_rise	LIN Rising Edge	Normal Mode; V_{BB} = 12 V			22.5	μs
T_sym	LIN Slope Symmetry	Normal Mode; V_{BB} = 12 V	−4	0	4	μs
LIN Receiver						
Trec_prop_down	Propagation Delay of Receiver Falling Edge		0.1		6	μs
Trec_prop_up	Propagation Delay of Receiver Rising Edge		0.1		6	μs
Trec_sym	Propagation Delay Symmetry	Trec_prop_down − Trec_prop_up	−2		2	μs
MODE TRANSITIONS TIMEOUTS						
T_LIN_wake	Duration of LIN Dominant for Detection of wake−up via LIN bus	Sleep Mode	30	90	150	μs
T_WAKE	Duration of Low level on WAKE Pin for local wakeup detection	Sleep Mode	7		50	μs
T_enable	Duration of High Level on EN Pin for Transition to Normal Mode		2	5	10	μs
T_disable	Duration of Low Level on EN Pin for Transition to Sleep Mode		2	5	10	μs
T_TxD_timeout	TxD Dominant Time−Out	Normal Mode, TxD = low, Guarantees Baudrate as Low as 1 kbps	15		50	ms

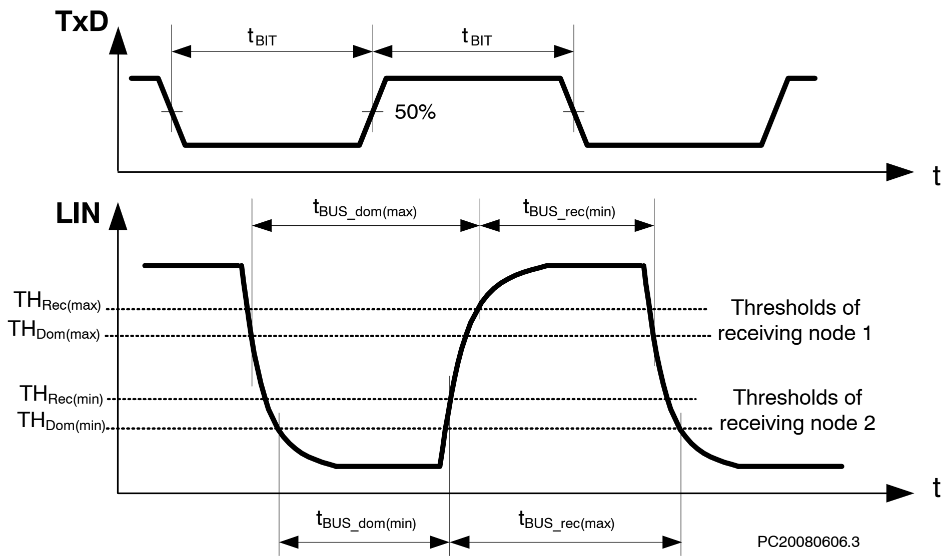


Figure 6. LIN Transmitter Duty Cycle

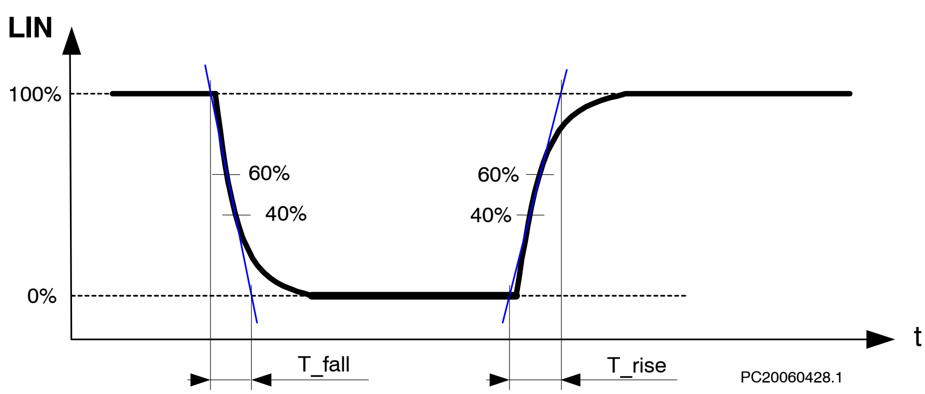


Figure 7. LIN Transmitter Rising and Falling Times

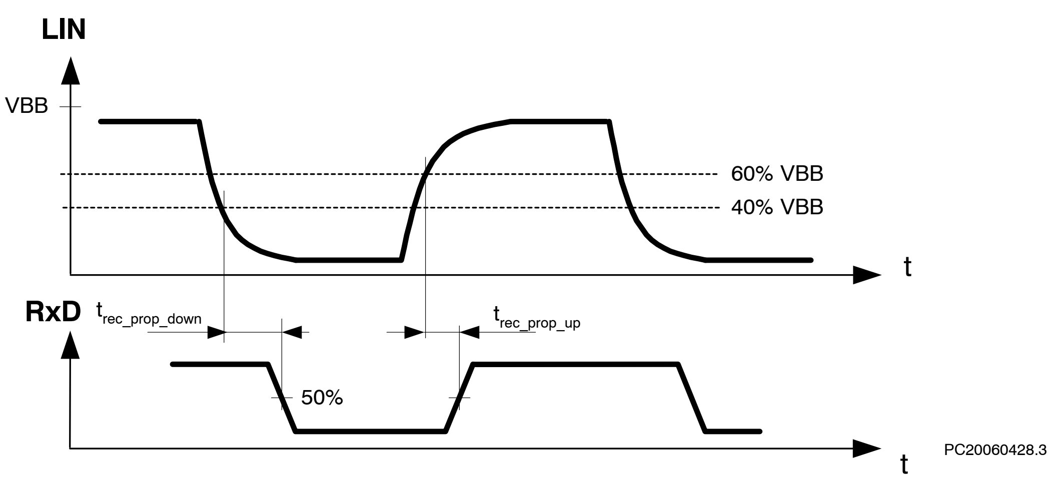


Figure 8. LIN Receiver Timing

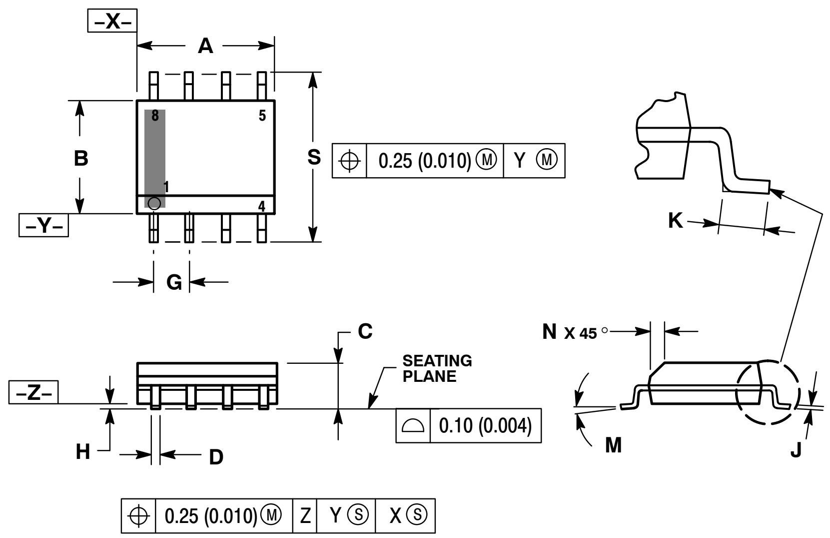
DEVICE ORDERING INFORMATION

Part Number	Version	Temperature Range	Package Type	Shipping†
NCV7321D10G	Stand−alone LIN Transceiver	−40°C − 125°C	SOIC−8 (Pb−Free)	96 Tube / Tray
NCV7321D10R2G				3000 / Tape & Reel
NCV7321D11G	Improved Stand−alone LIN Transceiver (In Development)			96 Tube / Tray
NCV7321D11R2G				3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

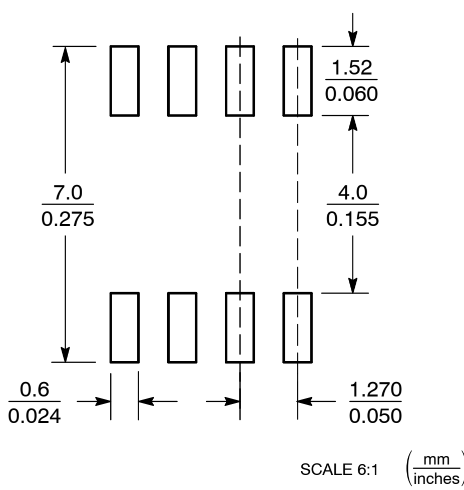
SOIC−8 NB
CASE 751−07
ISSUE AJ



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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